REMARKS

Claims 1-8 are pending in the present application. Claims 9-12 have been added.

Entry of the above amendments is earnestly solicited. An early and favorable first action on the merits is earnestly requested.

Should there be any matters that need to be resolved in the present application, the Examiner is respectfully requested to contact OSRAM SYLVANIA at (978) 777-1900.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE."

Respectfully submitted,

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_____
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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE ABSTRACT OF THE DISCLOSURE:

      The Abstract of the Disclosure has been amended as follows:

Abstract of the Disclosure

[Drive for a half-bridge inverter]

The selection of the dead time in the case of a half-bridge inverter influences the efficiency thereof. The optimal dead time, and thus the optimal switching-on time of a lower half-bridge transistor (T2) is accomplished according to the invention by virtue of the fact that switching on is delayed until the current in a level shift transistor (T3) has dropped below a given threshold. A further aspect of the invention consists in that the delay in switching on the lower half-bridge transistor (T2) is immediately suppressed whenever a charging current flows in a trapezoidal capacitor, and this is accompanied by the rise of the half-bridge output voltage (UHB) after the traversal of a minimum.

[Figure 4]

IN THE CLAIMS:

      The claims have been amended as follows:

6. (Amended) The half-bridge inverter as claimed in <u>claim 2</u> [one of claims 2-5], wherein a trapezoidal capacitor is coupled to the working electrode of the lower half-bridge switch , and the blocking of the control input of the interruption initiation switch is cancelled by an apparatus, which acquires the current through the trapezoidal capacitor , when the current flows from the working electrode of the lower half-bridge switch to the trapezoidal capacitor .

7. (Amended) The half-bridge inverter as claimed in claim 4 [or 5], wherein the series circuit of two diodes (D4, D5) is connected in parallel with the current negative feedback network , and a trapezoidal capacitor is connected between the connecting point of the diodes and the working electrode of the lower half-bridge switch , the diodes being polarized such that a current that flows from the working electrode of the lower half-bridge switch into the trapezoidal capacitor flows through the current negative feedback network .

Abstract of the Disclosure

The selection of the dead time in the case of a half-bridge inverter influences the efficiency thereof. The optimal dead time, and thus the optimal switching-on time of a lower half-bridge transistor (T2) is accomplished according to the invention by virtue of the fact that switching on is delayed until the current in a level shift transistor (T3) has dropped below a given threshold. A further aspect of the invention consists in that the delay in switching on the lower half-bridge transistor (T2) is immediately suppressed whenever a charging current flows in a trapezoidal capacitor, and this is accompanied by the rise of the half-bridge output voltage (UHB) after the traversal of a minimum.